UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,494	09/15/2003	Howard E. Rhodes	M4065.0087/P087-A	7413

24998 7590 10/26/2007

DICKSTEIN SHAPIRO LLP
1825 EYE STREET NW
Washington, DC 20006-5403

EXAMINER	
BERARDESCA, PAUL M	

ART UNIT	PAPER NUMBER
4115	

MAIL DATE	DELIVERY MODE
10/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/661,494	RHODES, HOWARD E.	
	Examiner	Art Unit	
	Paul Berardesca	4115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *80-96* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *80-96* is/are rejected.

7)☒ Claim(s) *80 and 84* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 80 is objected to because of the following informalities: In line 4, the term "the array" has no antecedent basis and is assumed to mean an array; in line 8, the term "the pixel array" has no antecedent basis and is assumed to mean "the array". Appropriate correction is required.

Claim 84 is objected to because of the following informalities: In line 6, the term "the array" has no antecedent basis and is assumed to mean an array; in line 9, the term "the pixel array" has no antecedent basis and is assumed to mean "the array". Appropriate correction is required.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422

F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 80 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 6,654,057. Although the conflicting claims are not identical, they are not patentably distinct from each other because although claim 1 of application includes a first and second pixel while claim 14 of U.S. Patent claim includes a first and second sensor, a pixel is a type of sensor, in addition claim 14 includes ***"a sensor array having rows and columns of pixel sensors"*** in the preamble therefore ***"sensor"*** and ***"pixel sensor"*** reads on ***"pixel"***.

In addition, claim 80 of application includes ***"the array comprising the first and second pixels"*** in the body and claim 14 of U.S. Patent includes ***"a sensor array having rows and columns of pixel sensors on a substrate wherein two adjacent pixel sensors in a row are connected"*** in the preamble, which reads on ***"the array comprising the first and second pixels"*** and ***"pixel sensors"*** read on ***"pixels."***

In addition, line 6 of claim 1 of application states, ***"detecting a first voltage level at a node of the first pixel"*** while claim 14 of U.S. Patent states, ***"detecting a first voltage at a node of a respective activated sensor"*** wherein ***"respective activated sensor"*** reads on ***"the first pixel"*** on the basis of the above analysis and ***"voltage"*** reads on ***"voltage level."***

In addition, lines 7-9 of claim 1 of application state, ***"resetting the first voltage level of the node to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array"*** while claim 14 of U.S. Patent states, ***"resetting the voltage of the respective nodes of said activated sensors to a predetermined voltage, wherein said voltage is reset by a reset transistor addressed by a reset line which is linear in said substrate."*** Although claim 14 does not specifically say ***"the first voltage level of the node", "the voltage of the respective nodes of said activated sensors"*** includes the voltage of both nodes, wherein ***"voltage"*** and ***"voltage level"*** are equivalent. In addition, ***"using a reset transistor" (claim 1)*** reads on ***"wherein said voltage is reset by a reset transistor" (claim 14)***. In addition, claim 1 includes ***"reset line that extends approximately linearly across the pixel array"*** while claim 14 includes ***"a reset line which is linear in said substrate."*** However, claim 14 states in the preamble ***"a sensor array having rows and columns of pixel sensors on a substrate wherein two adjacent pixel sensors in a row are connected",*** therefore if the reset line is linear in the substrate it must be linear in the pixel array and ***"linear in said substrate"*** reads on ***"approximately linearly across the pixel array".***

In addition, line 10 of claim 1 of application states, ***"transferring charge collected by the first pixel to the node"*** while claim 14 states, ***"transferring electrical charges collected by said activated sensor to said node"*** wherein ***"electrical charges"*** read on ***"charges"*** and ***"said activated sensor"*** reads on ***"the first pixel"*** based on the above analysis, and ***"said node"*** reads on ***"the node".***

In addition, line 11 of claim 1 of application states, ***"detecting the charge at the node"*** while claim 14 of U.S. Patent states, ***"detecting a second voltage at said node".*** A ***"second voltage"*** reads on ***"charge"*** because claim 14 states, ***"each sensor capable of collecting electric charge"*** and therefore a charge must be detected if a second voltage is detected.

In addition, line 12 of claim 1 of application states, ***"the shared column line"*** which reads on claim 14 of U.S. Patent, which states, ***"said shared column line."***

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 14 for the purpose of making the claim terminology more clear and concise.

Claim 81 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 6,654,057. Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference between the two is claim 81 says, ***"the shared column line extends approximately linearly across the pixel array"*** while claim 18 says, ***"said shared column line is linear in said substrate".*** However, as stated above, because independent claim 14 states, ***"a sensor array having rows and columns of pixel sensors on a substrate"*** the array is on the substrate and therefore if a column line is linear in the substrate it must be linear across the pixel array and therefore claim 81 is anticipated by claim 18.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 18 for the purpose of clearly claiming the structure of the array in light of the specification.

Claim 83 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 21 of U.S. Patent No. 6,654,057. Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference between the two is claim 83 says, ***"a row select line that extends approximately linearly across the pixel array"*** while claim 21 says, ***"said row select transistor is addressed by a row select line which is linear in said substrate".*** However, as stated above, because claim 14 states, ***"a sensor array having rows and columns of pixel sensors on a substrate"*** the array is on the substrate and therefore if a row select line is linear in the substrate it must be linear across the pixel array. In addition, even though claim 83 is broader than claim 21, all of the limitations of claim 83 are anticipated by claim 21.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 14 for the purpose of simplifying the claim language.

Claim 84 rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 14 of U.S. Patent No. 6,654,057. Although the conflicting claims are not identical, they are not patentably distinct from each other because although claim 84 states, ***"focusing an image on an active pixel CMOS***

imager, the imager comprising a pixel array" and claim 14 states, ***"an image focused on a sensor array",*** but claim 14 fails to disclose "***an active pixel CMOS imager"*** the specification discloses that the sensor array is a CMOS sensor array and therefore is an obvious variant thereof.

In addition, although claim 84 of application includes a first and second pixel while claim 14 of U.S. Patent claim includes a first and second sensor, a pixel is a type of sensor, in addition claim 14 includes ***"a sensor array having rows and columns of pixel sensors"*** in the preamble therefore ***"sensor"*** and ***"pixel sensor"*** reads on ***"pixel"***. In addition, claim 80 of application includes ***"the array comprising the first and second pixels"*** in the body and claim 14 of U.S. Patent includes ***"a sensor array having rows and columns of pixel sensors on a substrate wherein two adjacent pixel sensors in a row are connected"*** in the preamble, wherein ***"a sensor array having rows and columns of pixel sensors on a substrate wherein two adjacent pixel sensors in a row are connected"*** reads on ***"the array comprising the first and second pixels"*** and ***"pixel sensors"*** read on ***"pixels."***

In addition, claim 84 of application states, ***"detecting a first voltage level at a node associated with the first pixel"*** while claim 14 of U.S. Patent states, ***"detecting a first voltage at a node of a respective activated sensor"*** wherein ***"respective activated sensor"*** reads on ***"the first pixel"*** on the basis of the above analysis.

In addition, claim 84 of application states, ***"resetting the first voltage level of the node to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array"*** while claim 14 of

U.S. Patent states, ***"resetting the voltage of the respective nodes of said activated sensors to a predetermined voltage, wherein said voltage is reset by a reset transistor addressed by a reset line which is linear in said substrate."*** Although claim 14 does not specifically say ***"the first voltage level of the node", "the voltage of the respective nodes of said activated sensors"*** includes the voltage of both nodes, wherein ***"voltage"*** and ***"voltage level"*** are equivalent. In addition, ***"using a reset transistor" (claim 1)*** reads on ***"wherein said voltage is reset by a reset transistor" (claim 14)***. In addition, claim 1 includes ***"reset line that extends approximately linearly across the pixel array"*** while claim 14 includes ***"a reset line which is linear in said substrate."*** However, claim 14 states in the preamble ***"a sensor array having rows and columns of pixel sensors on a substrate wherein two adjacent pixel sensors in a row are connected",*** therefore if the reset line is linear in the substrate it must be linear in the pixel array and ***"linear in said substrate"*** reads on ***"approximately linearly across the pixel array".***

In addition, claim 84 of application states, ***"transferring charge collected by the first pixel to the node"*** while claim 14 states, ***"transferring electrical charges collected by said activated sensor to said node"*** wherein ***"electrical charges"*** read on ***"charges"*** and ***"said activated sensor"*** reads on ***"the first pixel"*** based on the above analysis, and ***"said node"*** reads on ***"the node".***

In addition, claim 84 of application states, ***"detecting the charge at the node"*** while claim 14 of U.S. Patent states, ***"detecting a second voltage at said node".*** A ***"second voltage"*** reads on ***"charge"*** because claim 14 states, ***"each sensor capable***

of collecting electric charge" and therefore a charge must be detected if a second voltage is detected.

In addition, claim 84 of application states, ***"the shared column line, the output signal corresponding to the image",*** which reads on claim 14 of U.S. Patent, which states, ***"said shared column line."*** In addition, claim 14 states, ***"generating an output signal corresponding to an image"*** which reads on ***"the output signal corresponding to the image."***

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 14 for the purpose of making the claims more clear and concise in light of the invention.

Claim 85 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 6,654,057. Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference between the two is claim 85 says, ***"the shared column line extends approximately linearly across the pixel array"*** while claim 18 says, ***"said shared column line is linear in said substrate".*** However, as stated above, because independent claim 14 states, ***"a sensor array having rows and columns of pixel sensors on a substrate"*** the array is on the substrate and therefore if a column line is linear in the substrate it must be linear across the pixel array and therefore claim 85 is anticipated by claim 18.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 85 for the purpose of making the claim more clear in light of the specification.

Claim 87 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 21 of U.S. Patent No. 6,654,057. Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference between the two is claim 87 says, ***"a row select line that extends approximately linearly across the pixel array"*** while claim 21 says, ***"said row select transistor is addressed by a row select line which is linear in said substrate".*** However, as stated above, because claim 14 states, ***"a sensor array having rows and columns of pixel sensors on a substrate"*** the array is on the substrate and therefore if a row select line is linear in the substrate it must be linear across the pixel array. In addition, even though claim 87 is broader than claim 21, all of the limitations of claim 87 are anticipated by claim 21.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 87 for the purpose of making the claim more clear in light of the specification.

Claim 88 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 33 of U.S. Patent No. 6,654,057. Although the conflicting claims are not identical, they are not patentably distinct from each other

because the only differences between the two claims are that claim 33 includes ***"a plurality of CMOS imager pixels for generating"*** while claim 88 includes, ***"a plurality of pixels to generate"*** wherein claim 88 is broader than claim 33 simply because it does not include that the pixels are CMOS pixels. In addition, claim 33 includes ***"output signals generated from detected light"*** while claim 88 includes, ***"to output the signal".*** Therefore claim 88 is broader than claim 33 simply because it does not include that the output signals are generated from detected light.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 88 for the purpose of simplifying the claim language.

Claim 89 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 35 of U.S. Patent No. 6,654,057. Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference between the two claims is that claim 35 states, ***"column line is linear in said array"*** while claim 89 states, ***"column lines extend approximately linear across array"***, wherein ***"in said array"*** reads on ***"across array",*** therefore, claim 89 is broader than claim 35 simply because it states "***approximately."***

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 88 for the purpose of broadening the claim.

Claim 91 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 37 of U.S. Patent No. 6,654,057. Although the conflicting claims are not identical, they are not patentably distinct from each other because the only difference between the two claims is that claim 37 states, ***"odd row lines and even row lines are is linear in said array"*** while claim 91 states, ***"odd and even row select lines extend approximately linearly"***, wherein ***"in said array"*** reads on ***"across array"***, therefore, claim 91 is broader than claim 37 simply because it states "***approximately.***"

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify claim 88 for the purpose of broadening the claim with ***"approximately."***

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 80-83 and 88-96 are rejected under 35 U.S.C. 102(b) as being anticipated by Bird US Patent 5,721,422).

Regarding claim 80, Bird discloses electronic devices having an array with shared column conductors.

Specifically, Bird discloses in the time interval A, the –5 volt row pulse is applied to only the row conductor (21a) of the row N and pixels (10A) and (10B) are connected to the row conductor (21a) and the reference conductor (1) of pixel (10A) is biased to a less negative voltage (-2.5V) than the row pulse (-5V) so the rectifying elements (S1) and (S2) of pixel (10A) are forward biased and so the capacitance of photodiode (8) of pixel (10A) is recharged and its residual charge read out via the shared column conductor (11a), which reads on claimed, ***"activating a first pixel in a row connected to a shared column line for a first period of time",*** as disclosed in column 6 lines 29-40 and exhibited in figures 1 and 2 wherein pixel (10A) reads on claimed, ***"first pixel."*** In addition, Bird discloses in the time interval B, the row pulse is again applied to row conductor (21a) of row N, but the reference conductor (1) is at –7.5V so that the rectifying elements (S1) and (S2) of pixel (10B) are forward-biased so the photodiode (8) of pixel (10B) is read out and re-charged, which reads on claimed, ***"and then subsequently activating an adjacent second pixel in the row connected to the shared column line for a second period of time, the array comprising the first and second pixels",*** as disclosed in column 6 lines 40-50 and exhibited in figures 1 and 2, wherein pixel (10B) reads on claimed, ***"second pixel."***

In addition, Bird discloses the capacitance of photodiode (8) of pixel (10A) is recharged and its residual charge is read out via the shared column conductor (11a), which reads on claimed, ***"detecting a first voltage level at a node of the first pixel",*** as disclosed in column 6 lines 29-40 and exhibited in figures 1 and 2, wherein the point

on the column conductor (11a) between the two pixels (10A) and (10B) as shown in figure 1 reads on claimed, ***"node."***

In addition, Bird discloses after the first time interval (A) (when the rectifying elements (S1) and (S2) of pixel (10A) are forward-biased and the capacitance of photodiode (8) of pixel (10A) is recharged and read out), the pulse applied to row conductor (21a) from the row driving circuit (60) is set to 0V and the pulse applied to the conductor (1) is set to -2.5V. Therefore, the reference conductor (1) is set to a lower voltage than the row pulse so the rectifying elements (S1) and (S2) are reverse-biased and therefore set the node between the two photodiodes (8) to a predetermined voltage, wherein the row pulse is governed by a row driving circuit (60) containing switching of transistor switches on each row conductor (21) and the reference conductor (1) is governed by transistor switches (57) and (58), wherein the lines associated with each of the transistors are extended linearly across the pixel array, which reads on claimed, ***"resetting the first voltage level of the node to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array",*** as disclosed in column 5 lines 30-41 and 50-67 and column 6 lines 13-28 and exhibited in figures 1, 2, and 7, wherein the switching transistors (57) and (58) read on claimed, ***"reset transistor",*** and the reference conductors (1, 2, 3, and 4) read on claimed, ***"reset line."*** Bird inherently discloses resetting the first voltage level of the node to a predetermined voltage because every time a sequential read out of the pixel (10A) is performed the row conductor (21a) is set to –5V and the reference conductor (1) is set to –7.5V thus turning on the rectifying elements (S1) and

(S2), but when the pixel (10A') is read out, the row conductor (21a) is set to 0V, therefore at this point, the voltage level of the node is set to a predetermined voltage governed by the row conductor (21a) being 0V.

In addition, Bird discloses a row pulse is applied to the row conductor (21a) of the row N including pixel (10A) and when the pulse is –5V the rectifying elements (S1) and (S2) are forward biased so the capacitance of photodiode (8) of pixel (10A) is recharged and the charge is read out at the node via the shared column conductor (11a), therefore the charge is transferred from the photodiode (8) to the node, which reads on claimed, ***"transferring charge collected by the first pixel to the node; detecting the charge at the node; and generating an output signal over the shared column line",*** as disclosed in column 6 lines 13-30 and exhibited in figures 1 and 2.

Regarding claim 81, Bird discloses everything claimed as applied above (see claim 1). Specifically, Bird discloses the column line (11a) extends linearly from the top of the array to the bottom of the array, which reads on claimed, ***"the shared column line extends approximately linearly across the pixel array"***, as exhibited in figure 1.

Regarding claim 82, Bird discloses everything claimed as applied above (see claim 81). Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, ***"further comprising a row select line that extends approximately linearly across the pixel***

array", as disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-line reads on claimed, ***"row select line."***

Regarding claim 83, Bird discloses everything claimed as applied above (see claim 80). Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, ***"further comprising a row select line that extends approximately linearly across the pixel array"***, as disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-line reads on claimed, ***"row select line."***

Regarding claim 88, Bird discloses electronic devices having an array with shared column conductors.

Specifically, Bird discloses an array of pixels, which reads on claimed, ***"plurality of pixels"***, as disclosed in column 4 lines 53-55 and exhibited in figure1; wherein the pixels are read in a known manner by an output circuit (70) and are eventually from an output (71) to an appropriate store or display wherein each pixel contains a photosensitive element (8) which store charge in response to light incident on the element (8) wherein the pixels are arranged in rows and columns of an array, which reads on claimed, ***"to generate an output signal associated with detected light, the plurality of pixels arranged in rows and columns of an array"***,, as disclosed in column 4 lines 64-68 and column 8 lines 15-20 and exhibited in figures 1 and 7.

In addition, Bird discloses a plurality of column lines each connected to at least two adjacent pixels of a row in the array, the column lines connected to the output circuit (70) to the output signal (71), which reads on claimed, ***"a plurality of column lines each connected to at least two adjacent pixels of a row in the array, the column lines being connected to output circuitry to output the signal",*** as exhibited in figure 7.

In addition, Bird discloses the row conductors (21) are scan lines for scanning the pixels of the sensor array on a row by row basis and they are orthogonal to the column lines and address both the odd and even pixels in the rows, which reads on claimed, ***"a plurality of odd row select lines orthogonal to the column lines to address odd pixels in the rows",*** and claimed, ***"a plurality of even row select lines orthogonal to the column lines to address even pixels in the rows",*** as disclosed in column 4 lines 55-58 and exhibited in figures 1 and 7, wherein the odd row conductors (21a) read on claimed, ***"odd row select lines"*** and the even row conductors (21b) reads on claimed, ***"even row select lines."***

In addition, Bird discloses a column drive circuitry (70) which is used to select the pixels connected to the column lines, which reads on claimed, ***"a column driver to address pixels connected to the column lines",*** as disclosed in column 6 lines 59-64 and exhibited in figures 1 and 7.

In addition, Bird discloses a row drive circuit (60) used to scan pixels of the sensor array on a row by row basis, scanning even and odd rows, which reads on claimed, ***"a row driver to address pixels through the odd row select lines and the***

even row select lines", as disclosed in column 4 lines 54-58 and exhibited in figures 1 and 7.

Regarding claim 89, Bird discloses everything claimed as applied above (see claim 88). Specifically, Bird discloses the column line (11a) extends linearly from the top of the array to the bottom of the array, which reads on claimed, ***"the column lines extend approximately linearly across the array"***, as exhibited in figure 1.

Regarding claim 90, Bird discloses everything claimed as applied above (see claim 89). Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, ***"the odd and even row select lines extend approximately linearly across the array"***, as disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-lines read on claimed, ***"odd and even row select lines."***

Regarding claim 91, Bird discloses everything claimed as applied above (see claim 88). Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, ***"the odd and even row select lines extend approximately linearly across the array"***, as

disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-lines read on claimed, ***"odd and even row select lines."***

Regarding claim 92, Bird discloses everything claimed as applied above (see claim 88). Specifically, Bird discloses that the reference conductors (1) and (2) are used to reset the pixels after they have been read by reverse-biasing their corresponding rectifying elements (S1) and (S2) using the timing sequence shown in figure 2 wherein the reference conductors (1) and (2) are linear across the array, which reads on claimed, ***"a plurality of reset lines that extend approximately linearly across the array"***, as disclosed in column 5 lines 17-40 and exhibited in figure 1 and 2.

Regarding claim 93, Bird discloses a read-out circuit for active matrix imaging arrays.

Specifically, Bird discloses a row driver circuit (60) is coupled to row conductors (21) and generates pulses using the row conductors (21) as scan lines for scanning the pixels of the sensor array on a row by row basis wherein the scan lines are orthogonal to column lines and address both the odd and even pixels in the rows which reads on claimed, ***"addressing even pixels in a row of pixels of an array of pixels using a row driver coupled to an even row select line",*** as disclosed in column 4 lines 55-60 and exhibited in figures 1 and 7, wherein the even row conductors (21b) read on claimed, ***"even row select line."***

In addition, Bird discloses the sensing elements (8) are photosensitive diodes which are contained in each pixel (10) wherein the photosensing element (8) is able to store charge in response to light incident on the element (8) wherein the change in charge state of the photodiode (8) at the end of the integration period is read out on the column conductor (11), which reads on claimed, ***"providing a first output signal associated with light detected by the even pixels to a plurality of column lines coupled to the even pixels; addressing odd pixels in the row of pixels via an even row select line",*** as disclosed in column 4 lines 60-65 and column 5 lines 45-50 and exhibited in figures 1 and 7, wherein the change in charge state of the even photodiodes (8) reads on claimed, ***"a first output signal."***

In addition, Bird discloses a row driver circuit (60) is coupled to row conductors (21) and generates pulses using the row conductors (21) as scan lines for scanning the pixels of the sensor array on a row by row basis wherein the scan lines are orthogonal to column lines and address both the odd and even pixels in the rows which reads on claimed, ***"addressing odd pixels in a row of pixels via an even row select line",*** as disclosed in column 4 lines 55-60 and exhibited in figures 1 and 7, wherein the even row conductors (21b) read on claimed, ***"even row select line."***

In addition, Bird discloses the sensing elements (8) are photosensitive diodes which are contained in each pixel (10) wherein the photosensing element (8) is able to store charge in response to light incident on the element (8) wherein the change in charge state of the photodiode (8) at the end of the integration period is read out on the column conductor (11), which reads on claimed, ***"providing a first output signal***

associated with light detected by the even pixels to a plurality of column lines coupled to the even pixels; addressing odd pixels in the row of pixels via an even row select line", as disclosed in column 4 lines 60-65 and column 5 lines 45-50 and exhibited in figures 1 and 7, wherein the change in charge state of the odd photodiodes (8) reads on claimed, ***"a first output signal."***

Regarding claim 94, Bird discloses everything claimed as applied above (see claim 93). Specifically, Bird discloses the column lines (11) are linear across the array and orthogonal to the row conductors (21), which reads on claimed, ***"the column lines extend approximately linearly across the array and are approximately orthogonal to both the even row select line and the odd row select line"***, as exhibited in figure 1. Because the row conductors (21) address even and odd pixels the odd row conductors (21a) read on claimed, ***"odd row select line"*** and the even row conductors (21b) reads on claimed, ***"even row select line."***

Regarding claim 95, Bird discloses everything claimed as applied above (see claim 94). Specifically, Bird discloses the odd row conductors (21a) and the even row conductors (21b) extend linearly across the array, which reads on claimed, ***"the odd and even row select lines extend approximately linearly across the array"***, as exhibited in figure 1.

Regarding claim 96, Bird discloses everything claimed as applied above (see claim 94). Bird discloses after the first time interval (A) (when the rectifying elements (S1) and (S2) of pixel (10A) are forward-biased and the capacitance of photodiode (8) of pixel (10A) is recharged and read out), the pulse applied to row conductor (21a) from the row driving circuit (60) is set to 0V and the pulse applied to the conductor (1) is set to -2.5V. Therefore, the reference conductor (1) is set to a lower voltage than the row pulse so the rectifying elements (S1) and (S2) are reverse-biased and therefore set the node between the two photodiodes (8) to a predetermined voltage, wherein the row pulse is governed by a row driving circuit (60) containing switching of transistor switches on each row conductor (21) and the reference conductor (1) is governed by transistor switches (57) and (58), wherein the lines associated with each of the transistors are extended linearly across the pixel array, which reads on claimed, ***"a plurality of reset lines that extend approximately linearly across the array",*** as disclosed in column 5 lines 30-41 and 50-67 and column 6 lines 13-28 and exhibited in figures 1, 2, and 7 wherein the reference conductors (1, 2, 3 and 4) read on claimed, ***"reset lines."***

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 84 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bird in view of Ackland et al. (US Patent 5,576,763) hereinafter referenced as Ackland.

Regarding claim 84, Bird discloses electronic devices having an array with shared column conductors. In addition, Bird discloses in the time interval A, the –5 volt row pulse is applied to only the row conductor (21a) of the row N and pixels (10A) and (10B) are connected to the row conductor (21a) and the reference conductor (1) of pixel (10A) is biased to a less negative voltage (-2.5V) than the row pulse (-5V) so the rectifying elements (S1) and (S2) of pixel (10A) are forward biased and so the capacitance of photodiode (8) of pixel (10A) is recharged and its residual charge read out via the shared column conductor (11a), which reads on claimed, ***"activating a first pixel in a row connected to a shared column line for a first period of time",*** as disclosed in column 6 lines 29-40 and exhibited in figures 1 and 2 wherein pixel (10A) reads on claimed, ***"first pixel."*** In addition, Bird discloses in the time interval B, the row pulse is again applied to row conductor (21a) of row N, but the reference conductor (1) is at –7.5V so that the rectifying elements (S1) and (S2) of pixel (10B) are forward-biased so the photodiode (8) of pixel (10B) is read out and re-charged, which reads on claimed, ***"and then subsequently activating an adjacent second pixel in the row connected to the shared column line for a second period of time, the array comprising the first and second pixels",*** as disclosed in column 6 lines 40-50 and exhibited in figures 1 and 2, wherein pixel (10B) reads on claimed, ***"second pixel."***

In addition, Bird discloses the capacitance of photodiode (8) of pixel (10A) is recharged and its residual charge is read out via the shared column conductor (11a), which reads on claimed, ***"detecting a first voltage level at a node of the first pixel",*** as disclosed in column 6 lines 29-40 and exhibited in figures 1 and 2, wherein the point on the column conductor (11a) between the two pixels (10A) and (10B) as shown in figure 1 reads on claimed, ***"node."***

In addition, Bird discloses after the first time interval (A) (when the rectifying elements (S1) and (S2) of pixel (10A) are forward-biased and the capacitance of photodiode (8) of pixel (10A) is recharged and read out), the pulse applied to row conductor (21a) from the row driving circuit (60) is set to 0V and the pulse applied to the conductor (1) is set to -2.5V. Therefore, the reference conductor (1) is set to a lower voltage than the row pulse so the rectifying elements (S1) and (S2) are reverse-biased and therefore set the node between the two photodiodes (8) to a predetermined voltage, wherein the row pulse is governed by a row driving circuit (60) containing switching of transistor switches on each row conductor (21) and the reference conductor (1) is governed by transistor switches (57) and (58), wherein the lines associated with each of the transistors are extended linearly across the pixel array, which reads on claimed, ***"resetting the first voltage level of the node to a predetermined voltage using a reset transistor addressed by a reset line that extends approximately linearly across the pixel array",*** as disclosed in column 5 lines 30-41 and 50-67 and column 6 lines 13-28 and exhibited in figures 1, 2, and 7, wherein the switching transistors (57) and (58) read on claimed, ***"reset transistor",*** and the reference conductors (1, 2, 3,

and 4) read on claimed, ***"reset line",*** and Bird inherently discloses resetting the first voltage level of the node to a predetermined voltage because every time a sequential read out of the pixel (10A) is performed the row conductor (21a) is set to –5V and the reference conductor (1) is set to –7.5V thus turning on the rectifying elements (S1) and (S2), but when the pixel (10A') is read out, the row conductor (21a) is set to 0V, therefore at this point, the voltage level of the node is set to a predetermined voltage governed by the row conductor (21a) being 0V.

In addition, Bird discloses a row pulse is applied to the row conductor (21a) of the row N including pixel (10A) and when the pulse is –5V the rectifying elements (S1) and (S2) are forward biased so the capacitance of photodiode (8) of pixel (10A) is recharged and the charge is read out at the node via the shared column conductor (11a), therefore the charge is transferred from the photodiode (8) to the node, which reads on claimed, ***"transferring charge collected by the first pixel to the node; detecting the charge at the node; and generating an output signal over the shared column line",*** as disclosed in column 6 lines 13-30 and exhibited in figures 1 and 2.

In addition, Bird discloses the device elements (8) may be photosensitive elements of an image sensor device, wherein the image sensor device has an array of pixels (10), which reads on claimed, ***"the imager comprising a pixel array",*** as disclosed in column 4 lines 51-55 and exhibited in figures 1 and 3, however, Bird fails to disclose "***focusing an image on an active pixel CMOS imager***". However, the examiner maintains that it was well known in the art to provide "***focusing an image on an active pixel CMOS imager***", as taught by Ackland.

In addition, Ackland discloses a single-polysilicon CMOS active pixel. In addition, Ackland discloses a plurality of single polysilicon active pixels (36) arranged to form an imaging array which may be used as a solid–state camera and in an exemplary imaging array, one or more signal timing controllers may be employed to sequentially activate the pixels in each row generating a serial video signal corresponding to an image focused on the array, which reads on claimed, ***"focusing an image on an active pixel CMOS imager",*** as disclosed in column 6 lines 61-67.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Bird by specifically providing "***focusing an image on an active pixel CMOS imager"***, as taught by Ackland, for the purpose of forming an active pixel using a process wherein only one polysilicon deposition is required, as disclosed in column 1 lines 54-60 and to be used as a solid-state camera as disclosed in column 6 lines 61-67.

Regarding claim 85, Bird and Ackland, the combination, discloses everything claimed as applied above (see claim 84), in addition, Bird discloses ***"The method of claim 84, wherein the shared column line extends approximately linearly across the pixel array."*** Specifically, Bird discloses the column line (11a) extends linearly from the top of the array to the bottom of the array, which reads on claimed, ***"the shared column line extends approximately linearly across the pixel array"***, as exhibited in figure 1.

Regarding claim 86, Bird and Ackland, the combination, discloses everything claimed as applied above (see claim 81), in addition, Bird discloses ***"The method of claim 85, further comprising a row select line that extends approximately linearly across the pixel array."*** Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, ***"further comprising a row select line that extends approximately linearly across the pixel array"***, as disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-line reads on claimed, ***"row select line."***

Regarding claim 87, Bird and Ackland, the combination, discloses everything claimed as applied above (see claim 80), in addition, Bird discloses ***"The method of claim 84, further comprising a row select line that extends approximately linearly across the pixel array."*** Specifically, Bird discloses row conductors (21) are scan-lines for addressing rows of the display elements sequentially on a row by row basis wherein the row conductors extend linearly across the pixel array, which reads on claimed, ***"further comprising a row select line that extends approximately linearly across the pixel array"***, as disclosed in column 12 lines 38-40 and exhibited in figure 1, wherein the scan-line reads on claimed, ***"row select line."***

Conclusion

Any inquiry concerning this communication or earlier cornmunications from the examiner should be directed to Paul Berardesca whose telephone number is (571) 270-3579. The examiner can normally be reached on Mon- Fri 7:30am-5:00pm EST (Alternate Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jefferey Harold can be reached on (571)272-7519. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Berardesca
Examiner
Art Unit 4115

PB

RYAN YANG 10/24/07
PRIMARY EXAMINER